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461 GI-cube: an architecture for volumetric global illumination and rendering

Frank Dachille, IX, Arie Kaufman

August 2000 HWWS '00: Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware

Publisher: ACM

The power and utility of volume rendering is increased by global illumination. We present a hardware architecture, GI-Cube, designed to accelerate volume rendering, empower volumetric global illumination, and enable a host of ray-based volumetric processing. ...

Keywords: hardware accelerator, volume processing, volume rendering, volumetric global illumination, volumetric ray tracing

462 The click modular router

Eddie Kohler, Robert Morris, Benjie Chen, John Jannotti, M. Frans Kaashoek
August 2000 ACM Transactions on Computer Systems (TOCS), Volume 18 Issue 3
Publisher: ACM
Full text available: pdf(376.31 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 31, Downloads (12 Months): 216, Citation Count: 137

Clicks is a new software architecture for building flexible and configurable routers. A Click router is assembled from packet processing modules called elements. Individual elements implement simple router functions like packet classification, ...

Keywords: component systems, routers, software router performance

463 Power-optimal encoding for DRAM address bus (poster session)

Wei-Chung Cheng, Massoud Pedram
August 2000 ISLPED '00: Proceedings of the 2000 international symposium on Low power electronics and design
Publisher: ACM
Full text available: pdf(207.02 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 10, Citation Count: 7

This paper presents Pyramid code, an optimal code for transmitting sequential addresses over a DRAM bus. Constructed by finding an Eulerian cycle on a complete graph, this code is optimal for conventional DRAM in the sense that it minimizes the switching ...

464 On-chip vs. off-chip memory: the data partitioning problem in embedded processor-based systems

Preeti Ranjan Panda, Nikil D. Dutt, Alexandru Nicolau
July 2000 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 5 Issue 3
Publisher: ACM
Full text available: pdf(175.91 KB) Additional Information: full citation, abstract, references, cited by, index terms, review

Bibliometrics: Downloads (6 Weeks): 59, Downloads (12 Months): 246, Citation Count: 18

Efficient utilization of on-chip memory space is extremely important in modern embedded system applications based on processor cores. In addition to a data cache that interfaces with slower off-chip memory, a fast on-chip SRAM, called Scratch-Pad memory, ...

Keywords: data cache, data partitioning, memory synthesis, on-chip memory, scratch-pad memory, system design, system synthesis

465 Piranha: a scalable architecture based on single-chip multiprocessing

Luiz André Barroso, Kourosh Gharachorloo, Robert McNamara, Andreas Nowatzyk, Shaz Qadeer, Barton Sano, Scott Smith, Robert Stets, Ben Verghese

June 2000 ISCA '00: Proceedings of the 27th annual international symposium on Computer architecture

Publisher: ACM

Full text available: pdf(191.10 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 27, Downloads (12 Months): 180, Citation Count: 84

The microprocessor industry is currently struggling with higher development costs and longer design times that arise from exceedingly complex processors that are pushing the limits of instruction-level parallelism. Meanwhile, such designs are especially ...

466 Hardware implementation of communication protocols modeled by concurrent EFSMs with multi-way synchronization

Hisaaki Katagiri, Keiichi Yasumoto, Akira Kitajima, Teruo Higashino, Kenichi Taniguchi

June 2000 DAC '00: Proceedings of the 37th conference on Design automation

Publisher: ACM

Full text available: pdf(123.98 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 14, Citation Count: 1

In this paper, we propose a technique to implement communication protocols as hardware circuits using a model of concurrent EFSMs with multi-way synchronization. Since use of multi-way synchronization enables simple and comprehensible specifications ...

Keywords: LOTOS, communication protocols, concurrent EFSMs, high-level synthesis, mutli-way synchronization

467 Bus encoding for low-power high-performance memory systems

Naehyuck Chang, Kwanho Kim, Jinsung Cho

June 2000 DAC '00: Proceedings of the 37th conference on Design automation

Publisher: ACM

Full text available: pdf(132.11 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 28, Citation Count: 8

High-performance memory buses consume large energy as they include termination networks, BiCMOS and/or open-drain output. This paper introduces power reduction techniques for memory systems deliberating on burst-mode transfers over the high-speed bus ...

468 Naming as a fundamental concept of open hypermedia systems

Manolis Tzagarakis, Nikos Karousos, Dimitris Christodoulakis, Siegfried Reich
May 2000 HYPERTEXT '00: Proceedings of the eleventh ACM on Hypertext and hypermedia
Publisher: ACM
Full text available: pdf(125.38 KB) Additional Information: full citation, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 20, Citation Count: 5

Keywords: component-based open hypermedia system (CB-OHS), naming system, reference architecture

469 Parameterized system design

Tony D. Givargis, Frank Vahid
May 2000 CODES '00: Proceedings of the eighth international workshop on Hardware/software codesign
Publisher: ACM
Full text available: pdf(101.74 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 9, Citation Count: 5

Continued growth in chip capacity has led to new methodologies stressing reuse, not only of pre-designed processing components, but even of entire pre-designed architectures. To be used across a variety of applications, such architectures must ...

Keywords: cache, estimation, intellectual property, low power, on-chip bus, system parameters, system-on-a-chip

470 Piranha: a scalable architecture based on single-chip multiprocessing

Luiz André Barroso, Kourosh Gharachorloo, Robert McNamara, Andreas Nowatzyk, Shaz Qadeer, Barton Sano, Scott Smith, Robert Stets, Ben Verghese
May 2000 ACM SIGARCH Computer Architecture News, Volume 28 Issue 2
Publisher: ACM
Full text available: pdf(191.10 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 27, Downloads (12 Months): 180, Citation Count: 84

The microprocessor industry is currently struggling with higher development costs and longer design times that arise from exceedingly complex processors that are pushing the limits of instruction-level parallelism. Meanwhile, such designs are especially ...

471 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli
April 2000 ACM Transactions on Design Automation of Electronic Systems (TODAES), Volume 5 Issue 2
Publisher: ACM
Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 37, Downloads (12 Months): 569, Citation Count: 68

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, ...

472 CyPhone—bringing augmented reality to next generation mobile phones

Tino Pyssysalo, Tapio Repo, Tuukka Turunen, Teemu Lankila, Juha Röning
April 2000 DARE '00: Proceedings of DARE 2000 on Designing augmented reality environments
Publisher: ACM
Full text available: pdf(6.46 MB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 15, Downloads (12 Months): 144, Citation Count: 0

We describe a prototype implementation of a future mobile phone called CyPhone. In addition to voice calls, it has been designed to support context-specific and multi-user multimedia services in an augmented reality manner. Context-awareness has been ...

Keywords: mobile communication, navigation, networked virtual reality, real-time data transport protocols, registration

473 Narrow bus encoding for low power systems

Youngsoo Shin, Kiyoung Choi
January 2000 ASP-DAC '00: Proceedings of the 2000 conference on Asia South Pacific design automation
Publisher: ACM
Full text available: pdf(72.43 KB) Additional Information: full citation, references, cited by

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 23, Citation Count: 4

474 A hybrid approach for core-based system-level power modeling

Tony Givargis, Frank Vahid, Jörg Henkel
January 2000 ASP-DAC '00: Proceedings of the 2000 conference on Asia South Pacific design automation
Publisher: ACM
Full text available: pdf(128.11 KB) Additional Information: full citation, references, cited by
Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 23, Citation Count: 8

475 Applying packet techniques to cellular radio

N. F. Maxemchuk
December 1999 Wireless Networks, Volume 5 Issue 6
Publisher: Kluwer Academic Publishers
Full text available: pdf(310.07 KB) Additional Information: full citation, references, index terms
Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 28, Citation Count: 0

476 Pre-Fetching for Improved Core Interfacing

Roman Lysecky, Frank Vahid, Tony Givargis, Rilesh Patel
November 1999 ISSS '99: Proceedings of the 12th international symposium on System synthesis
Publisher: IEEE Computer Society
Full text available: pdf(127.99 KB) Publisher Site Additional Information: full citation, abstract, references, cited by
Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 4, Citation Count: 4

Reuse of cores can reduce design time for systems-on-a-chip. Such reuse is dependent on being able to easily interface a core to any bus. To enable such interfacing, many propose separating a core's interface from its internals. However, this separation ...

Keywords: Cores, system-on-a-chip, interfacing, on-chip bus, intellectual property

477 MIL primitives for querying a fragmented world

Peter A. Boncz, Martin L. Kersten
October 1999 The VLDB Journal — The International Journal on Very Large Data Bases, Volume 8 Issue 2
Publisher: Springer-Verlag New York, Inc.
Full text available: pdf(261.36 KB) Additional Information: full citation, abstract, references, cited by, index terms
Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 36, Citation Count: 13

In query-intensive database application areas, like decision support and data mining, systems that use vertical fragmentation have a significant performance advantage. In order to support relational or object oriented applications on top of such a fragmented ...

Keywords: Database systems, Main-memory techniques, Query languages, Query optimization, Vertical fragmentation

478 Optimization of mesh locality for transparent vertex caching

Hugues Hoppe
July 1999 SIGGRAPH '99: Proceedings of the 26th annual conference on Computer graphics and interactive techniques
Publisher: ACM Press/Addison-Wesley Publishing Co.
Full text available: pdf(2.46 MB) Additional Information: full citation, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 45, Citation Count: 21

Keywords: geometry compression, triangle strips

479 Functional verification of the equator MAP1000 microprocessor

Jian Shen, Jacob Abraham, Dave Baker, Tony Hurson, Martin Kinkade, Gregorio Gervasio, Chen-chau Chu, Guanghui Hu
June 1999 DAC '99: Proceedings of the 36th ACM/IEEE conference on Design automation
Publisher: ACM
Full text available: pdf(73.73 KB) Additional Information: full citation, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 22, Citation Count: 6

480 A methodology for the verification of a "system on chip"

Daniel Geist, Giora Biran, Tamara Arons, Michael Slavkin, Yvgeny Nustov, Monica Farkas, Karen Holtz, Andy Long, Dave King, Steve Barret
June 1999 DAC '99: Proceedings of the 36th ACM/IEEE conference on Design automation
Publisher: ACM
Full text available: pdf(63.75 KB) Additional Information: full citation, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 33, Citation Count: 2

Keywords: systems on chip, test and debugging, verification

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